Work for Digital Electronics Supervision II

The questions below are partitioned into two sets: the *core* questions and the *extension* questions. The core questions are based on material that the course should have covered by the end of lecture 6, and you should be familiar with. Nevertheless, they will likely take a bit of thought. All of the past Tripos questions set in the work are attached at the end of this document.

The extension questions are based on the same material, but will take longer, and require a lot more thought. Attempting them is optional. The more of the extension questions that you try, the better you will become at Digital Electronics and the easier you will find the work in future weeks. However, do not sacrifice your progress in other subjects or your health for the sake of completing them.

Please attempt all four core items and as many of the extension questions as you can, and send your work to me by 1800 on Friday, 24th October. All your answers, working and any additional thoughts should be written up in LaTeX and emailed to `mti20@cam.ac.uk`.

Core questions

1. Examples sheet questions 8, 10, 13, 14, 16.

   For 10, also write down the propagation delay and contamination delay of the circuit.

2. What is the difference between a flip flop and a latch? Give an example (or two) of the use of each. How might a flip flop be constructed from a latch?

3. Examination question: 1995 Paper 2 Question 22.

4. Examination question: 1997 Paper 2 Question 2 (first three parts only).

   For the second part, please include a schematic diagram and ensure to include thorough explanations of the setup time, hold time and the delay from a clock edge to the output. What relation should hold between two of these quantities to provide sensible behaviour and why? What happens if setup time or hold time are violated? How could such violations occur? Comment on the possibility and desirability of negative hold times. It may help to include a timing diagram to illustrate your answer.

   For the third part, ensure to give a concrete example after your explanation.

Extension questions

5. Design an asynchronous circuit with inputs A and B and output Y that has the following truth table:

A	B	Y_t
0	0	0
0	1	Y_{t-1}
1	0	Y_{t-1}
1	1	1

   where Y_{t-1} denotes a *don't change* condition.

   That is, use RS latches and other components to design a circuit that:

   (a) reflects its inputs when the states of all the inputs match, and

   (b) whose output should remain in this state until the inputs all transition to the other state.

6. Examination question: 1996 Paper 2 Question 3.

7. Read about the operation of an Enigma machine, available at `http://en.wikipedia.org/wiki/Enigma_machine`. Pay special attention to the diagrams relating the inputs, outputs, rotors and reflector.

   Consider a cut-down Enigma machine, consisting of two rotors, that operates on an alphabet containing the characters A–D only. Choose the design of each rotor yourself. Give the state diagram of such an Enigma machine implemented as a Mealy machine. You may assume the state advances before input character is pressed.

   Note that, unlike that for a Moore machine, each *edge* in the state diagram for a Mealy machine is labelled with the value of the input and the value of the output. An example is given at `http://en.wikipedia.org/w/index.php?title=Mealy_machine&oldid=628793016#Examples`.

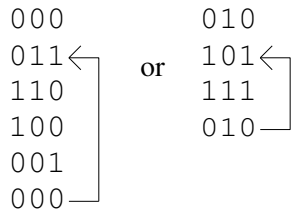
   Can you convert your Mealy machine into a Moore machine?

   Please include plenty of illustrations to make your method and choice of design decisions clear.

1995 Paper 2 Question 22

Digital Electronics and Computer Design

A sequential circuit has been built, and it behaves slightly erratically. When switched on it produces on its three output wires one of the following patterns:



The second pattern is not intended to arise. Deduce the circuit details and propose a modification that ensures that in due course the circuit will always settle into the cycle shown in the first pattern.

[20 marks]

1997 Paper 2 Question 2

Digital Electronics

What is a *don't care term* and how can such terms arise in practice? [5 marks]

Explain the operation of an edge triggered D-type flip flop, taking care to explain any timing constraints. [5 marks]

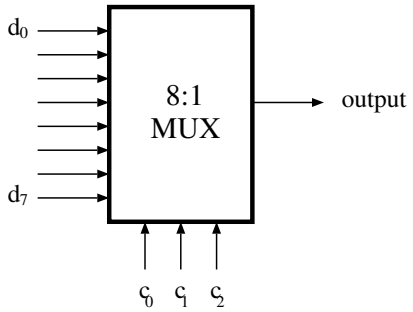
Explain the operation of a tristate output. How are such outputs used? [5 marks]

Give the circuit diagram for a CMOS tristate inverter. [5 marks]

1996 Paper 2 Question 3

Digital Electronics

(a) A multiplexer is a device that selects one of its inputs as the output. The selection is determined by a set of control signals. For example, in the 8:1 multiplexer shown below, the output will be equal to d_6 when $c_2 = 1$, $c_1 = 1$ and $c_0 = 0$.



Give a circuit which implements this 8:1 multiplexer using only NAND gates. [10 marks]

(b) Using only 8:1 multiplexers, show how to build a 16:1 multiplexer. [4 marks]

(c) Show how an 8:1 multiplexer and a single inverter can be used to implement any combinational function of four variables. (You may assume the availability of signals for logical 1 and logical 0.) [6 marks]