Work for Digital Electronics Supervision I

The questions below are partitioned into two sets: the *core* questions and the *extension* questions. The core questions are based on material that the course should have covered by the end of lecture 3, and you should be familiar with. Nevertheless, they will likely take a bit of thought.

The extension questions are based on the same material, but will take longer, and require a lot more thought. Attempting them is optional. The more of the extension questions that you try, the better you will become at Digital Electronics and the easier you will find the work in future weeks. However, do not sacrifice your progress in other subjects or your health for the sake of completing them.

Please attempt all three core items and as many of the extension questions as you can, and send your work to me by 1800 on Friday, 17th October. All your answers, working and any additional thoughts should be written up in LaTeX and emailed to `mti20@cam.ac.uk`.

Core questions

1. Examples sheet questions 1, 2, 6, 7 and 11.

   For 2, also show that $x + (\overline{x}.y) = x + y$.

   For 6, do both sum-of-products and product-of-sums forms, not just sum-of-products as it says on the sheet.

2. (a) Show that $(X + Y).(X + Z) = X + Y.Z$

   (b) Show that $(X + Y).\left(\overline{X} + Z\right) = X.Z + \overline{X}.Y$

   (c) Hence, or otherwise, simplify

   $$P = \left(A + B + \overline{C}\right).\left(A + B + D\right).\left(A + B + E\right).\left(A + \overline{D} + E\right).\left(\overline{A} + C\right)$$

3. Examination question: 2004 Paper 10 Question 1 (attached to this document as the final page).

Extension questions

4. Design and draw out a circuit to subtract a positive 3-bit binary number $a = a_2a_1a_0$ from the positive 3-bit binary number $b = b_2b_1b_0$ (in general, there are no constraints on the relative magnitudes of a and b).

5. (This question contains non-examinable content; it is designed to test your ability to apply what you have learnt in lectures to a new, unseen scenario.)

   Throughout lectures and your work so far, you have used a single bit to encode a logical 0 and logical 1. That is, we use a low voltage on a single wire to indicate a logical 0 and a high voltage on the same single wire to indicate a logical 1, as follows:

code Q_0	**meaning**
0	logical 0
1	logical 1

Suppose we now introduce a second wire into our encoding, to form a *dual-rail encoding*, as follows:

code Q_1Q_0	**meaning**
00	clear
01	logical 0
10	logical 1

In future weeks, we shall use the additional "clear" meaning to encode the validity of a signal. That is, we shall design circuits where the circuit itself is able to tell us whether the resulting value is valid, or still being computed within the system.

(a) Design an inverter circuit that works in this new *dual-rail* encoding. Recall that an inverter is a circuit that changes a logical 0 into a logical 1, and a logical 1 into a logical 0. It does not make sense for an inverter to modify the validity of a signal.

(b) Recall that a conventional half-adder computes the sum and carry bits given two single-bit inputs, A and B. It has the following truth table:

A	B	H	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

where H is the sum of A and B, and C is the carry bit.
In our new dual-rail encoding, observe that this truth table becomes:

A_1	A_0	B_1	B_0	H_1	H_0	C_1	C_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	1	0	1
0	1	1	0	1	0	0	1
1	0	0	0	0	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	0	1	1	0

Explain why the second and third lines of this truth table are correct, establish Boolean equations for H_1, H_0, C_1 and C_0, and hence draw a circuit for the new half-adder implementation in the *dual-rail* encoding.

(c) Compare the number of gates used in each implementation of the half adder (that is, the conventional implementation and the *dual-rail* version).

(d) Assuming for this supervision that all gates have an equal propagation delay (i.e. it takes T picoseconds for a signal to propagate through an AND gate, an OR gate, or a NOT gate), what is the maximum delay of each half adder implementation?

6. Hozier College is a constituent college of the University of Grantabridge. The Porters' Lodge at Hozier College contains two rooms: one that is visible to students and the public, and one that is concealed, that only the Porters may enter. For most of the day, the Porters are accustomed to napping in the latter of these rooms. However, there have recently been complaints about the lack of "portering" that is occuring in the College, so the Porters have

purchased a Porter-Poking-Machine (PPM) to wake them up when necessary. It is your job to design the circuit that activates the PPM.

You are supplied with 5 inputs:

(i) The plodge is non-empty ($\overline{U}$).

(ii) The fire alarm is not silent ($\overline{W}$).

(iii) The fellows are not happy (they need bringing more port from the cellar) ($\overline{X}$).

(iv) The students are not calm (they are rioting) ($\overline{Y}$).

(v) The post is all sorted (Z).

The PPM wakes the porter up when its input is low. It should wake the porters up when one or more of the following scenarios are true:

(i) The plodge is empty, BUT the fellows need more port, OR

(ii) The plodge has a student waiting in it AND the fire alarm is going off AND the students are rioting elsewhere in College, OR

(iii) The plodge has a student waiting in it AND the fire alarm is going off AND the post needs sorting, OR

(iv) The plodge has a student waiting in it AND the post needs sorting BUT the students are calm, OR

(v) The fellows are happy AND the fire alarm is going off AND there is a student waiting in the plodge.

Given the above information,

(a) Write down a Boolean expression for $\overline{P}$, i.e. a Boolean expression detailing when the PPM should be triggered. Don't try and simplify it yet, just copy the conditions verbatim from the outline above.

(b) What do you notice about the Boolean expression that you have just written down (hint: look at question 2)?

(c) Draw out a circuit for a minimised version of your PPM driver.

2004 Paper 10 Question 1

Digital Electronics

(a) What is DeMorgan's theorem? [4 marks]

(b) What are *minterms*, *essential terms* and *prime implicants*? [6 marks]

(c) What are the prime implicants, essential terms and minimum sum of products for $f = (a.b) \oplus (c + d)$? [6 marks]

(d) Whenever $g = a.b$ is true, if we do not care what the output of f is, determine the new minimum sum of products form for f. [4 marks]